AMENDMENTS TO THE CLAIMS

1-16. (Canceled)

17. (New) An image processing apparatus comprising:

direct memory access devices connected to busses, said busses being connected to memories,

wherein a data bus width for one of the busses is less than a data bus width for another of the busses, a data bus width for said another of the busses being less than a data bus width for a different one of the busses.

18. (New) The image processing apparatus as set forth in claim 17, wherein one of the memories is connected to said one of the busses, another of the memories is connected to said another of the busses, and a different one of the memories is connected to said different one of the busses.

19. (New) The image processing apparatus as set forth in claim 18, wherein one of the direct memory access devices is connected to said one of the busses, another of the direct memory access devices is connected to said another of the busses, and a different one of the direct memory access devices is connected to said different one of the busses.

20. (New) The image processing apparatus as set forth in claim 17, wherein a controlling circuit is connected to each of the direct memory access devices, said controlling circuit commanding said direct memory access devices to access addresses within said memories.

21. (New) The image processing apparatus as set forth in claim 20, wherein a central processing unit is connected to said one of the busses, said central processing unit commanding said controlling circuit to command said direct memory access devices.

22. (New) The image processing apparatus as set forth in claim 21, wherein said central processing unit is not connected to said another of the busses or said different one of the busses.

23. (New) The image processing apparatus as set forth in claim 21, wherein a processing circuit is connected to said each of the direct memory access devices, said controlling circuit being connected to said processing circuit.

24. (New) The image processing apparatus as set forth in claim 23, wherein said processing circuit is configured to receive image data from said memories.

25. (New) The image processing apparatus as set forth in claim 24, wherein an image stored is in one of the memories, said image data being a trimmed portion of said image.

26. (New) The image processing apparatus as set forth in claim 25, wherein columns of said image data are sequentially read from said one of the memories when said image data is said trimmed portion.

27. (New) The image processing apparatus as set forth in claim 24, wherein a display controller is configured to convert said image data into a drive signal for a display.

28. (New) The image processing apparatus as set forth in claim 27, wherein said processing circuit is connected to said display controller, said display controller being connected to said display.

29. (New) The image processing apparatus as set forth in claim 27, wherein said display is a liquid crystal display.

30. (New) The image processing apparatus as set forth in claim 17, wherein random access memory is connected to said one of the busses.

31. (New) The image processing apparatus as set forth in claim 17, wherein dynamic random access memory is connected to said another of the busses.

32. (New) The image processing apparatus as set forth in claim 17, wherein flash memory is connected to said different one of the busses.

33. (New) The image processing apparatus as set forth in claim 17, wherein said data bus width for said one of the busses is 16 bits.

34. (New) The image processing apparatus as set forth in claim 17, wherein said data bus width for said another of the busses is 32 bits.

35. (New) The image processing apparatus as set forth in claim 17, wherein said data bus width for said different one of the busses is 64 bits.